

STACKED MICROELECTRONIC DIES AND METHODS FOR STACKING MICROELECTRONIC DIES

TECHNICAL FIELD

[0001] The present invention relates to stacked microelectronic dies and methods for stacking microelectronic dies.

BACKGROUND OF THE INVENTION

[0002] Packaged microelectronic assemblies, such as memory chips and microprocessor chips, typically include a microelectronic device mounted to a substrate and encased in a plastic protective covering. The device includes functional features, such as memory cells, processor circuits, and interconnecting circuitry. The device also typically includes bond pads electrically coupled to the functional features. The bond pads are coupled to pins or other types of terminals that extend outside the protective covering for connecting the microelectronic device to buses, circuits and/or other microelectronic assemblies.

[0003] One conventional approach to reducing the surface area occupied by packaged microelectronic devices in compact electronic products is to stack one packaged device on another packaged device having an identical configuration. For example, as shown in Figure 1, an upper packaged microelectronic device 20b can be stacked on a lower packaged microelectronic device 20a (collectively referred to as packaged devices 20) and the assembly of packaged devices 20 can be attached to a printed circuit board (PCB) 30. Each packaged device 20 typically includes a die 24 encased in an encapsulant 23. Each die 24 has a plurality of die bond pads 25 connected to pins 43 that extend outside the encapsulant 23. Corresponding pins 43 of each packaged device 20 are connected directly to each other and to corresponding bond pads 31 on the PCB

30. The packaged devices 20 are also connected to each other by attaching an adhesive 11 between the encapsulant 23 of the lower packaged device 20a and the encapsulant 23 of the upper packaged device 20b.

[0004] In another conventional arrangement shown in Figure 2, two identical packaged devices 120 (shown as a lower packaged device 120a and an upper packaged device 120b) are connected to each other and to a PCB 130 with solder balls 143. Each packaged device 120 can include a die 124 mounted to a substrate PCB 140 and encased with an encapsulant 123. Each die 124 has die bond pads 125 connected with wire-bonds 126 to corresponding bond pads 131a of the substrate PCB 140. The bond pads 131a are connected to solder ball pads 131b with circuitry internal to the support PCB 140. The solder balls 143 connect the solder ball pads 131b of the upper package 120b to the solder ball pads 131b of the lower package 120a. Additional solder balls 143 connect the lower package 120a to corresponding bond pads 131c of the PCB 130.

[0005] One drawback with the conventional arrangements described above with reference to Figures 1 and 2 is that the stacked packaged devices are connected to each other. Accordingly, it can be difficult to remove and replace one packaged device without removing or damaging the other. Furthermore, this arrangement can require several tests to confirm that the packaged devices remain operable after each manufacturing step. For example, the packaged devices may be tested individually before they are coupled, then tested again after they are coupled to each other, and then tested yet again after the coupled packaged devices are mounted to the PCB. Each test can add to the time required to complete the final product, and can accordingly reduce the efficiency of the manufacturing process.

SUMMARY

[0006] The present invention is directed toward microelectronic package assemblies and methods for stacking packaged microelectronic devices. A method in accordance with one aspect of the invention includes positioning a first

packaged microelectronic device adjacent to a support member having support member circuitry, and coupling the first packaged device to a first portion of the support member circuitry. The first packaged microelectronic device includes a first microelectronic die at least partially encased in a first encapsulant to define a first package configuration. The method further includes positioning at least proximate to the first packaged device a second packaged microelectronic device having a second microelectronic die at least partially encased in a second encapsulant to define a second package configuration different than the first package configuration. The second packaged device is electrically coupled to a second portion of the support member circuitry, and the first packaged device is positioned between the support member and the second packaged device. In a further aspect of this embodiment, the second packaged microelectronic device can be connected to the support member without being connected to the first packaged microelectronic device. Accordingly, the second packaged microelectronic device package can be removed from the support member without removing the first packaged microelectronic device.

[0007] The invention is also directed toward an assembly of packaged microelectronic devices. The assembly can include a support member having support member circuitry, and a first packaged microelectronic device connected to at least one of the support member and the support member circuitry. The first packaged device has a first microelectronic die at least partially encased in a first encapsulant to define a first package configuration. The assembly can further include a second packaged microelectronic device connected to at least one of the support member and the support member circuitry with the first packaged device positioned between the support member and the second packaged device. The second packaged device has a second microelectronic die at least partially encased in a second encapsulant to define a second package configuration different than the first package configurations, and the second packaged device can be connected directly to the support member without being connected to the first packaged device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a partially schematic, cross-sectional side view of two packaged microelectronic devices stacked in accordance with the prior art.

[0009] Figure 2 is a partially schematic, cross-sectional side view of two packaged microelectronic devices stacked in accordance with another prior art arrangement.

[0010] Figure 3 is a partially schematic, cross-sectional side view of two packaged microelectronic devices stacked in accordance with an embodiment of the invention.

[0011] Figure 4 is a partially schematic, cross-sectional side view of two stacked packaged microelectronic devices attached to a support member with solder balls in accordance with another embodiment of the invention.

[0012] Figure 5 is a partially schematic, cross-sectional side view of an initially unpackaged microelectronic die stacked on a packaged microelectronic die in accordance with yet another embodiment of the invention.

DETAILED DESCRIPTION

[0013] The present disclosure describes microelectronic devices and methods for stacking such devices. Many specific details of certain embodiments of the invention are set forth in the following description and in Figures 3-5 to provide a thorough understanding of these embodiments. One skilled in the art, however, will understand that the present invention may have additional embodiments, or that the invention can be practiced without several of the details described below.

[0014] Figure 3 is a partially schematic, cross-sectional side view of a microelectronic device assembly 210 that includes two packaged microelectronic devices 220 that are individually attached to a support member 230 in accordance with an embodiment of the invention. In one aspect of this embodiment, the assembly 210 can include a lower packaged device 220a positioned between the support member 230 and an upper packaged device 220b. In a further aspect of this embodiment, the lower packaged device 220a and the upper packaged

device 220b can have different configurations. For example, the lower packaged device 220a can include a first microelectronic die 224a mounted to a package substrate 240 (such as a PCB). The microelectronic features (such as integrated circuits) of the first microelectronic die 224a can be electrically coupled to first connecting members 243a (such as solder balls) with circuitry internal to the first microelectronic die 224a and/or the substrate 240. The upper packaged device 220b can include a second microelectronic die 224b having internal microelectronic features electrically coupled to second connecting members 243b (such as leads or pins). Both the lower packaged device 220a and the upper packaged device 220b can include an encapsulating material 223 that at least partially encases the microelectronic dies 224a and 224b.

[0015] In one embodiment, the support member 230 can include a PCB having first bond pads 231a aligned with the first connecting members 243a of the lower packaged device 220a, and second bond pads 231b aligned with the second connecting members 243b of the second packaged device 220b. The bond pads 231a, 231b can be coupled to internal circuitry 232 of the support member 230. In one aspect of this embodiment, the internal circuitry 232 electrically couples the first bond pads 231a to the second bond pads 231b for coupling the lower packaged device 220a to the upper packaged device 220b. Alternatively, the first bond pads 231a can be electrically isolated from the second bond pads 231b. In either embodiment, the lower packaged device 220a can be structurally and electrically connected to the support member 230 by attaching the first connecting members 243a directly to the first bond pads 231a. The upper packaged device 220b can be structurally and electrically connected to the support member 230 by attaching the second connecting members 243b directly to the second bond pads 231b.

[0016] In one embodiment, the upper packaged device 220b can be separated from the lower packaged device 220a by a gap "G". Alternatively, the upper packaged device 220b can rest on the lower packaged device 220a, and in another alternative embodiment, the upper packaged device 220b can be

attached to the lower packaged device 220a. An advantage of spacing the upper packaged device 220b apart from the lower packaged device 220a is that heat can be more readily convected away from the lower surface of the upper packaged device 220b and the upper surface of the lower packaged device 220a.

[0017] In any of the embodiments described above with reference to Figure 3, the planform shape or "footprint" of the upper packaged device 220b in a plane generally parallel to the support member 230 can be different than the planform shape of the lower packaged device 220a. For example, in one embodiment, the upper packaged device 220b can have a first and second edges 221b, 222b that extend outwardly beyond corresponding first and second edges 221a, 222a of the lower packaged device 220a. Accordingly, the second connecting members 243b can extend from the upper packaged device 220b alongside the first and second edges 221a, 222a of the lower packaged device 220a to the support member 230. In other embodiments, the assembly 210 can have other arrangements in which the upper packaged device 220b has a different configuration than the lower packaged device 220a. For example, the upper packaged device 220b can have a smaller planform shape than the lower packaged device 220a, so long as the second connecting members 243b can extend around the first and second edges 221a, 222a of the lower packaged device 220a to contact the support member 230. In still further embodiments, the assembly 210 can include more than two packaged devices 220. For example, the assembly 210 can include three or more stacked packaged devices 220 with one or more of the packaged devices 220 connected to the support member 230 separately from the rest of the packaged devices 220.

[0018] In one aspect of an embodiment of the assembly 210 described above with reference to Figure 3, the first microelectronic die 224a and the second microelectronic die 224b can be identical, but the packaged device 220a and 220b can have different configurations so that the lower packaged device 220a can fit beneath the upper packaged device 220b. Alternatively, the first microelectronic die 224a in the lower packaged device 220a can be different than

the second microelectronic die 224b in the upper packaged device 220b. For example, the first microelectronic die 224a can have a different processor capability or a different memory capacity than the second microelectronic die 224b. Alternatively, the first and second microelectronic dies 224a, 224b can be functionally as well as configurationally distinct. For example, the first microelectronic die 224a can include a processor and the second microelectronic die 224b can include memory circuits.

[0019] One feature of an embodiment of the assembly 210 described above with reference to Figure 3 is that the lower packaged device 220a and the upper packaged device 220b are each individually electrically coupled to the support member 230. An advantage of this feature is that the test requirements for the assembly 210 and the components of the assembly 210 can be less than the test requirements for some conventional arrangements. For example, both the lower packaged device 220a and the upper packaged device 220b can each be tested individually only once before mounting the packaged devices 220 to the support member 230 and once after mounting. In one specific example, the lower packaged device 220a can be tested again after it is mounted to the support member 230, but before mounting the upper packaged device 220b to the support member 230. Accordingly, if the lower packaged device 220a fails the test, it can be serviced or replaced without disturbing the upper packaged device 220b. Alternatively, the upper packaged device 220b can be mounted to the support member 230 after mounting the lower packaged device 220a, but before testing the lower packaged device 220a. In either embodiment, the combination of the two packaged devices 220 need not be separately tested before mounting the packaged devices 220 to the support member because the packaged devices 220 are not directly electrically connected to each other before mounting, unlike some conventional arrangements such as those described above with reference to Figures 1 and 2.

[0020] Another feature of an embodiment of the assembly 210 described above with reference to Figure 3 is that the upper packaged device 220b can be

structurally separate from the lower packaged device 220a. An advantage of this feature is that the upper packaged device 220b can be separately removed from the support member 230 and replaced (if necessary) without adversely affecting the lower packaged device 220a. Accordingly, the assembly 210 can be less expensive and less time-consuming to maintain and repair.

[00221] Still another feature of an embodiment of the assembly 210 described above with reference to Figure 3 is that conventional techniques for attaching the packages to the support member 230 can be used. For example, conventional "pick and place" devices and methods that are typically used to position the lower packaged device 220a and the upper packaged device 220b on the support member 230 in a conventional unstacked arrangement can be used with little or no modification to stack the upper packaged device 220b over the lower packaged device 220a and attach both packaged devices 220 to the support member 230.

[0022] Figure 4 is a partially schematic, cross-sectional side view of a package assembly 310 having two packaged microelectronic devices 320 (shown as a lower packaged device 320a and an upper packaged device 320b) individually connected to a support member 330 with solder balls in accordance with another embodiment of the invention. In one aspect of this embodiment, each packaged device 320a, 320b includes a microelectronic die 324 mounted to a package substrate 340 (such as a printed circuit board), encased in an encapsulant 323, and electrically coupled to bond pads 341 of the package substrate 340. First solder balls 343a extend between the bond pads 341 of the lower packaged device 320 and corresponding first bond pads 331a of the support member 330. Second solder balls 343b extend between the bond pads 341 of the upper packaged device 320b and corresponding second bond pads 331b of the support member 330. The first bond pads 331a can be electrically coupled to the second bond pads 331b with circuitry internal to the support member 330, or alternatively, the first and second bond pads 331a, 331b can be electrically isolated, as described above with reference to Figure 3. In either embodiment, each

packaged device 320a, 320b is individually connected (both structurally and electrically) to the support member 330.

[0023] In other embodiments, the assembly 310 can have other configurations. For example, the lower packaged device 320a can be connected to the support member 330 with elongated conductive members (generally similar to the conductive members 243b described above with reference to Figure 3) instead of the first solder balls 343a. In still further embodiments, the lower packaged device 320a and/or the upper packaged device 320b can be connected to the support member 330 with other conductive members.

[0024] Figure 5 is a partially schematic, cross-sectional side view of a package assembly 410 that includes an initially unpackaged microelectronic die in accordance with an embodiment of the invention. In one aspect of this embodiment, the assembly 410 can include a packaged microelectronic device 420 having a first microelectronic die 424a mounted to a package substrate 440 and at least partially encased in a first encapsulating material 423a. The packaged device 420 is then coupled to first bond pads 431a of an assembly support member 430 (such as a PCB) with first conductive members 443a (such as solder balls). The assembly 410 can further include a second microelectronic die 424b mounted directly to the first encapsulating material 423a. The second microelectronic die 424b can be connected to corresponding second bond pads 431b of the assembly support member 430 with second conductive members 443b (such as pins).

[0025] In one aspect of an embodiment of the assembly 410 described above with reference to Figure 5, the second microelectronic die 424b can be encapsulated after it has been mounted to the packaged microelectronic device 420. For example, a small volume of a second encapsulating material 423b can be disposed around the upper microelectronic die 424b and a portion of the second connecting members 443b. Alternatively, a larger volume of a second encapsulating material 423c can be disposed over the entire assembly 410 to

cover the packaged device 420, the upper microelectronic substrate 424b and the second connecting members 443b.

[0026] In other embodiments, the assembly 410 can have other arrangements that include an initially unpackaged microelectronic die mounted directly to a packaged microelectronic die. For example, in one alternate embodiment, the second microelectronic die 424b can be electrically coupled to the packaged device 420 in addition to or in lieu of directly coupling the second microelectronic die 424b to the assembly support member 430. The second microelectronic die 424b can contact the packaged device 420 (as shown in Figure 5) or, alternatively, the second microelectronic die 424b can be separated from the packaged device 420 by a gap in a manner generally similar to that described above with reference to Figure 3. In still another alternative embodiment, the second microelectronic die 424b can be attached (for example, with an adhesive) to the packaged device 420. In yet another embodiment, the second encapsulating material 423b or 423c that encases the second microelectronic die 424b can be eliminated. In still a further embodiment, the relative positions of the second microelectronic die 424b and the packaged device 420 can be reversed so that the second microelectronic die 424b is positioned between the assembly support member 430 and the packaged device 420.

[0027] From the foregoing it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.